Implementation of 8 Channels Phase Conjugation on FPGA for Microwave Power Transmission

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***Abstract*— This paper presents a phase conjugation (PC) system for 8 channels microwave power transmission (MPT) application, operating at the frequency band 2.45 GHz, using a field programmable gate array (FPGA) and high-speed analog to digital converter (ADC) and digital to analog converter (DAC). PC algorithm is implemented using some digital logics on the FPGA and a small size buffer is used for data acquisition. In addition, in order to operate the MPT system at 2.45 GHz, an appropriate frequency planning of ADC and DAC is proposed. Typical type of patch antennas is used to verify the implemented system and from the measurement results, it works well as the MPT application.**

***Keywords*—MPT, FPGA, Digital Logic, PC, Power transfer efficiency (PTE).**

I. INTRODUCTION

In the field of MPT research, it is necessary to maximize the PTE. various studies have been conducted to increase the PTE including the TR method of reversing the time of received signals [1, 2]. The PC method, equal to the TR method for a monochromatic wave, has been demonstrated to be an optimum method for MPT in a radiative near-field region from an EM perspective and a network analysis perspective, respectively [3, 4].

The implementation of the PC algorithm can be done in a variety of ways in analog and digital domain and has been presented in a number of different groups [5]-[11]. In the analog domains, some methods have been suggested, typically, pon-type and Van-Atta structure [5]-[9]. However, it is a critical disadvantage that continuous pilot signal is always required because analog-based PC method immediately re-transmissions the conjugated received pilot signal.

On the other hand, PC systems implemented in the digital domain can capture the incoming pilot signals, so they do not need continuous pilot signals. There have been studies on software implementation of PC algorithm in processing units [10, 11]. However, memory for the data acquisition of the received pilot signal and additional command executions on the processor to perform PC are needed. Therefore, the system based on digital logics is better than above methods to implement the system that processes the pilot signals received in real time and captures only necessary information by tiny memory. Therefore, in this study, the 8 channel PC based MPT system operating at the frequency band 2.45 GHz is implemented on a field programmable gate array (FPGA) with high-speed analog to digital converter (ADC) and digital to analog converter (DAC). The system measurement is done using simple patch antennas.

II. CONFIGURATION OF THE MPT SYSTEM

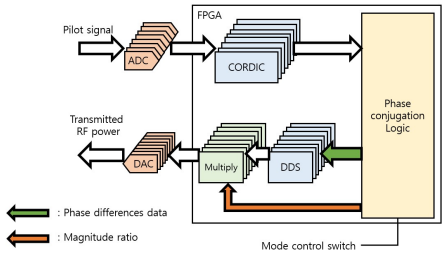

Fig. 1. Block diagram of the total WPT system

In order to implement the PC algorithm, the magnitude and phase information of the received pilot signal should be found. Xilinx's coordinate rotation digital computer (CORDIC) IP can find the magnitude and phase information of the received data. In addition, in order to reduce the noise term, moving average filter is applied with using Xilinx's finite impulse response (FIR) compiler IP. The calculated magnitude and phase data are utilized to find the phase differences and magnitude ratio and these data are captured in a buffer (e.g., first in first out (FIFO)). The transmit signal source is implemented by Xilinx's direct digital synthesizer (DDS) compiler. In order to implement the PC, magnitude ratio and phase differences of received pilot signal among 8 channels are utilized. Reversed phase differences data go to as DDS input and the magnitude ratio is multiplied with each DDS output, respectively. Fig. 1. shows the total MPT system block diagram. The calculation blocks of the magnitude ratio, phase differences, FIR compiler for moving average filter and buffer are integrated in the PC logic block. The external switch button is utilized to select between the pilot signal receiving mode and power transmission mode.

Numerically calculated oscillator (NCO) blocks and decimation or interpolation filters are integrated into each ADC and DAC block so that down-conversion or up-conversion can be implemented. Table 1. shows the ADC/DAC frequency planning including each frequency of NCO and decimation/interpolation factors. With this

setup, in the pilot signal receiving mode, 2.45 GHz RF signal is down-converted to 19.12 MHz in a digital domain. Similarly, the DDS output frequency is up-converted to 2.45 GHz by NCO frequency in the DAC block so as to RF power transmission. The proposed frequency planning table is just an example.

Table. 1. Frequency planning of the ADC and DAC.

	ADC	DAC
Sampling rate [GSPS]	1.47456	5.89824
NCO frequency [GHz]	0.430	2.250
Decimation or Interpolation	Decimation (factor 8)	Interpolation (factor 8)

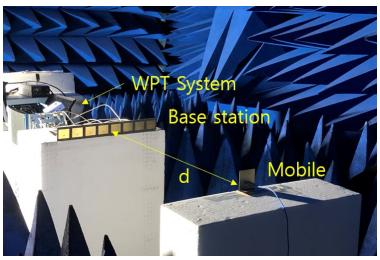

Fig. 2. The MPT measurement setup

III. SYSTEM MEASUREMENT

In order to verify the implemented system, the measurement is done using practical patch antenna operating at 2.45 GHz. 1 by 8 patch array antenna and a single patch antenna are used as the base station and mobile station, respectively. By changing the distance between the base station and the mobile, PTE is calculated by the measured data. Fig. 2. shows the setup environment of the MPT system. In order to compare to the simulation result, full wave commercial EM simulator (Altair FEKO) is performed. Fig. 3 shows PTE graph. The total system is simulated with 10 cm (0.8167λ) intervals from 20 cm (1.6333λ) to 140 cm (11.4333λ). The measurements are done at three points: 20 cm (1.6333λ), 50 cm (4.0833λ), and 100 cm (8.1667λ). Black solid line and red star dots show the calculated PTE from the simulation and measurement results, respectively. The measurement results show the well-matched tendencies with the simulation data so that implemented system well works as the MPT application.

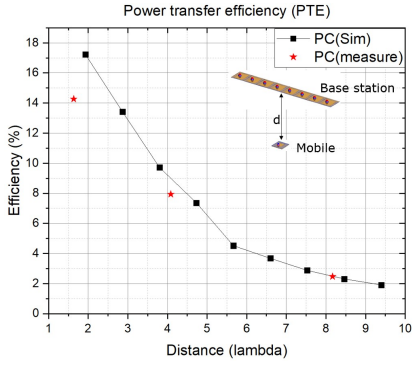

Fig. 3. PTE graph of the simulation and measurement

IV. CONCLUSION

In this paper, 8 channels PC system for MPT application operating at the frequency band 2.45 GHz is designed on hardware using the FPGA and high-speed ADC and DAC. Some digital logics are utilized, such as, CORDIC, DDS and FIR compiler and a small size of buffer is used for data acquisition. The advantages of this system are that it is possible to process the received pilot signal and capture only necessary data so that increase the processing speed and required memory is reduced. In order to operating the system at 2.45 GHz, proper frequency planning is suggested of ADC and DAC. The simple patch antennas are utilized so as to verify the system and it is confirmed that the system is applicable to the MPT system through the measurement results.

ACKNOWLEDGEMENT

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